PTO/SB/33 (07-05)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number: 07977-017002
I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, Box 1450, Alexandria, VA 22313-1450.	Application Number: 09/451,665	Filed: November 30, 1999
	First Named Inventor: Shunpei Yamazaki, et al.	
Date of Deposit	Art Unit: 2813	Examiner: Laura Schillinger
Signature		
Typed or Printed Name of Person Signing Certificate		

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☒ attorney or agent of record 37,640
(Reg. No.)

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Registration number if acting under 37 CFR 1.34 _____

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June 4, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ Total of 4 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Shunpei Yamazaki, et al.	Art Unit	: 2813
Serial No.	: 09/451,665	Examiner	: Laura Schillinger
Filed	: November 30, 1999	Conf. No.	: 9359
Title	: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Pursuant to United States Patent and Trademark Office OG Notices: 12 July 2005 - New Pre-Appeal Brief Conference Pilot Program, a request for a review of identified matters on appeal is hereby submitted with the Notice of Appeal. Review of these identified matters by a panel of examiners is requested because the rejections of record are clearly not proper and are without basis, in view of a clear legal or factual deficiency in the rejections. All rights to address additional matters on appeal in any subsequent appeal brief are hereby reserved.

Claims 1, 2, 4, 5, 7-13, 15, 16, 18-23, 25, 26, 28-34, 36, 37, 39-81 and 83 are pending. Claims 12, 13, 15, 16, 18-23, 25, 26, 28-34, 36, 37 and 39-81 have been withdrawn, leaving claims 1, 2, 4, 5, 7-11 and 83 under consideration with claim 1 being independent. Claims 1, 2, 4, 5 and 7-11 have been rejected as being anticipated by Farrenkopf (U.S. Patent No. 5,889,315). Claims 7 and 11 have been rejected as being unpatentable over Farrenkopf in view of Takemura (U.S. Patent No. 5,403,762).

Applicant specifically asks the panel to review the issues highlighted below.

1. Farrnekopf fails to describe or suggest forming a crystalline semiconductor film on an insulating surface, as recited in claim 1.

Claim 1 recites a method of manufacturing a semiconductor device by forming a crystalline semiconductor film on an insulating surface, forming an insulating film on the crystalline semiconductor film, and introducing a dopant impurity into the crystalline semiconductor film through the insulating film by ion doping. The crystalline semiconductor film then is annealed to repair lattice defects caused by the introduction of the dopant impurity, a gate electrode is formed over the insulating film, and a channel region is formed in the doped region of the crystalline semiconductor film. A peak of a concentration profile of the dopant impurity is located in the insulating film.

The Examiner has asserted that Farrnekopf's lower epitaxial layer 22 of Fig. 9I.2, which the Examiner equates with the recited substrate, is formed on an insulating surface. However, this is not the case. Rather, the layer 22 is formed on a conductive substrate 20 having a resistivity of 5-50 (typically 20) ohm-cm. See Farrenkopf at col. 8, lines 20-31.

In response to this argument, the Examiner has noted that, at col. 20, lines 50-60, and with reference to Fig. 9a, Fraunkopf describes forming a layer 150 of silicon oxide along the top of substrate region 20. However, at col. 21, lines 17-25, Farrenkopf states, with reference to Fig. 9e, that the oxide layer 150 is removed and epitaxial layer 22 is then deposited. Accordingly, the epitaxial layer 22 (which the Examiner equates with the crystalline semiconductor film recited in claim 1) cannot be said to be formed on the oxide layer. Thus, since epitaxial layer 22 is formed directly on the conductive substrate 20, formation of the epitaxial layer 22 does not constitute "forming a crystalline semiconductor film on an insulating surface," as recited in claim 1, and the rejection should be withdrawn.

2. Farrnekopf also fails to describe or suggest introducing a dopant impurity into the crystalline semiconductor film such that a peak of a concentration profile of the dopant impurity is located in an insulating film formed on the crystalline semiconductor film and over which a gate electrode is formed, as also recited in claim 1.

The Examiner asserts that Farrenkopf teaches introducing a dopant impurity through the oxide 168. However, the Examiner appears to ignore the further recitation in claim 1 that the dopant impurity is introduced into the crystalline semiconductor film (which the rejection equates with the lower epitaxial layer 22). Moreover, in presenting arguments about the concentration profile of the dopant impurity, the Examiner acknowledges that the dopant is not introduced into the layer 22.

In response to this argument, the Examiner states the following:

> Applicant argues that the impurities are not introduced into the crystalline semiconductor insulating film – however this is not persuasive because the mask oxide has holes which expose the layer to impurities.

As best understood, this argument is to the effect that introducing an impurity through holes in the oxide 168 constitutes introducing a dopant "through" the insulating film such that a peak of a concentration profile of the dopant impurity is located in the insulating film, as recited in claim 1. Applicant disagrees, since introducing the dopant through a region that does not include the oxide 168 does not constitute introducing "through" the oxide 168.

Moreover, the oxide 168 cannot constitute the insulating film recited in claim 1 since, as noted by Farrenkopf at col. 22, line 25, the oxide 168 is removed. As such, the oxide 168 cannot be said to be an insulating film over which a gate electrode is formed, as recited in claim 1.

For at least these additional reasons, the rejection should be withdrawn.

3. Takemura does not remedy the failure of Farrenkopf to describe or suggest the subject matter of the independent claims, and the rejection does not assert otherwise.

Takemura, which is cited as showing the use of diborane gas and irradiating a laser light to the crystalline semiconductor film, does not remedy the failures of Farrenkopf. Accordingly, the rejection of claims 7 and 11 also should be withdrawn.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 6/4/07

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